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Development of a Voltage Feedback Spice Op-Amp Macromodel

Introduction

A voltage-feedback amplifier macromodel has been developed that simulates the most common effects, such as transient response, frequency response, voltage noise and input/output slew rate limiting. Detailed descriptions of each stage in the model will be presented with examples of model performance and correlation to actual device behavior.

Macromodels are developed for the customer instead of releasing full transistor schematics. Of course, the most accurate simulations are conducted from fully-extracted 3-D device models. Not only would it be impractical to share these models because of the need to accommodate the numerous simulation platforms, but also because of proprietary reasons.

One of the first op-amp macromodel techniques was developed by Boyle in 1974 and used only two transistors, a few diodes and linear elements [1]. Linear elements like resistors, capacitors, inductor and voltage/current control sources simulate much faster than active elements and are used to provide poles, zeros and any gain. For a DC model, a voltage-controlled voltage source can represent the amplifier while resistances can be added to better represent the input and output impedance. Capacitors, inductors, diodes and transistors can then provide the proper AC response. If you want more information on the development of simulation models, see Alexander and Bowers [2] and [3]. We will follow their model here.

The ISL28133

As an example, we are going to investigate the ISL28133. The ISL28133 is a zero-drift operational amplifier with voltage feedback topology. Intended for low frequency and power precision applications, the gain bandwidth product is 400kHz, the slew rate is 0.1V/µs and the supply current is 18µA. A five-stage model represents the actual circuit, the block diagram for which is shown in Figure 1. They are the input stage, the gain stage, the frequency-shaping stage, the output stage and the noise module.

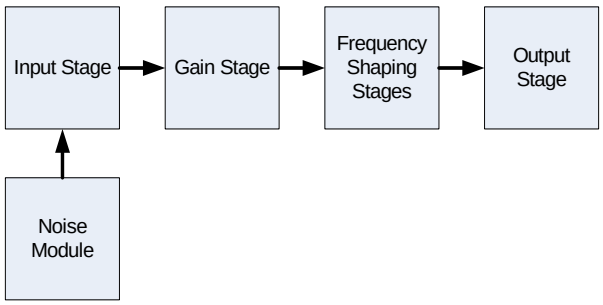

FIGURE 1. THE BLOCK DIAGRAM OF ISL28133 MACROMODEL

The Input Stage

The input stage of the zero-drift amplifier is shown in Figure 2. The 100µA current source 'I2' feeds the PMOS input pair. Normally, I2 should be chosen less than the quiescent current. Remember, the ISL28133's typical supply current (RL = open) is only 18µA. However, a small I2 (~10µA) would make the input voltage noise too large to emulate. This will be discussed later in the noise analysis part. Choose I2 = 100µA and use I1 to compensate back to the total quiescent current. Cin1 and Cin2 are the input common mode capacitance and Cdiff is the input differential mode capacitance.

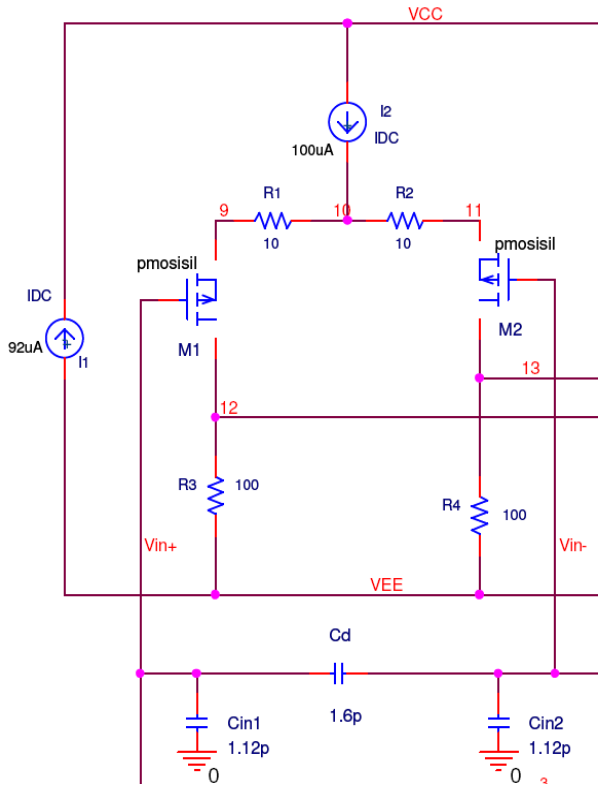

FIGURE 2. INPUT STAGE

The Gain Stage (Figure 3)

This stage performs some important functions in the model:

1. This stage sets the DC gain of the part. All the subsequent stages provide unity DC gain.
2. It provides slew rate limiting.
3. It adds the dominant pole to the AC characteristic.
4. It level shifts the signal from two voltages referred to the supplies to a single voltage referred to the mid-point.
5. It limits the full scale output swing.

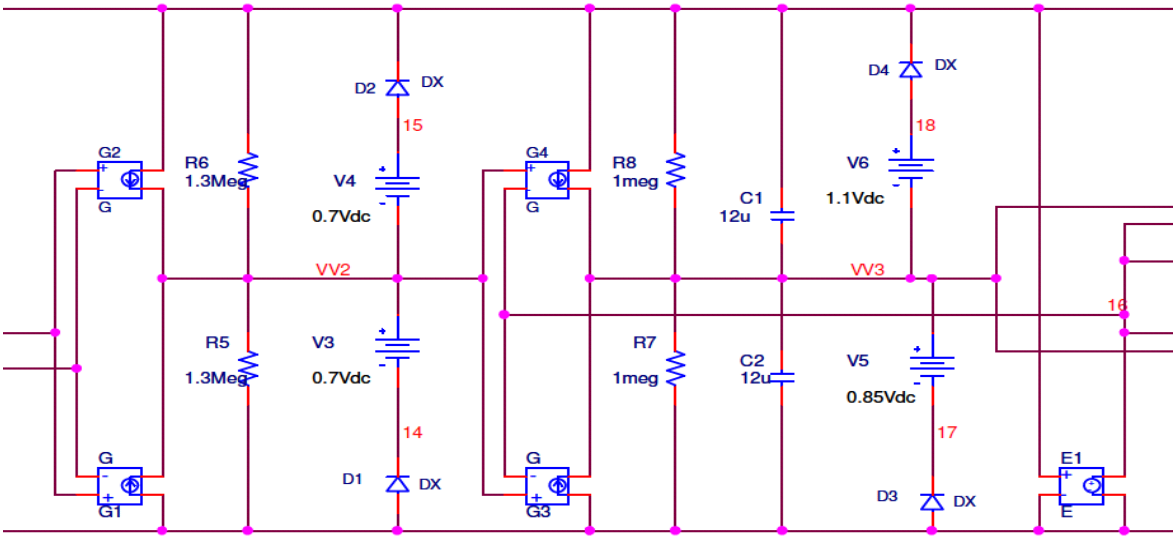

FIGURE 3. GAIN STAGE

Referring to Figure 3, Ga is the gain of block G1 and G2. Gb is the gain of block G3 and G4.

$$SlewRate = \frac{I2 \bullet R3 \bullet Ga \bullet R5 \bullet Gb}{C1} \quad \text{(EQ. 1)}$$

Changing the value of V3 and V4 limits the slew rate. Also, R8/C1 and R7/C2 decide the dominant pole of this model. E1 is used to set the reference level at the middle of Vcc and Vee.

Frequency-Shaping Stages

The "telescopic" frequency shaping techniques used here are very common in op-amp modeling. It is easy to add more poles and zeros. Each frequency-shaping block provides unity gain. A zero-pole pair is included in this model and shown in Figure 4.

$$R10 = R11 = 1M\Omega \quad \text{(EQ. 2)}$$

$$R9 = R12 = R10 \cdot (\frac{f_p}{f_z} - 1) \quad \text{(EQ. 3)}$$

$$L1 = L2 = \frac{R9}{2\pi f_p} \quad \text{(EQ. 4)}$$

A higher order pole stage is shown in Figure 5, G7/8, R13/14 and C3/4.

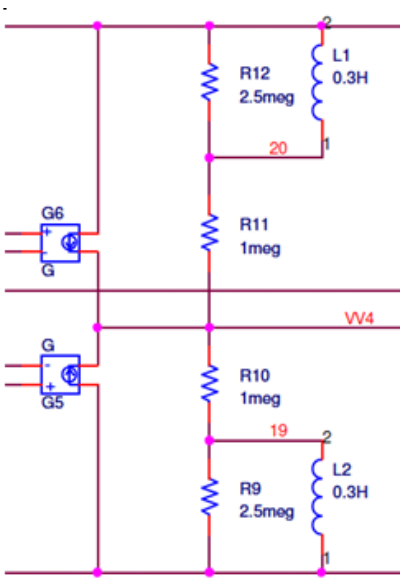

FIGURE 4. ZERO-POLE PAIR STAGE

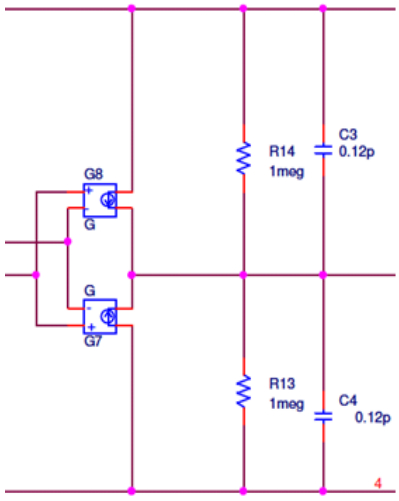

FIGURE 5. HIGHER ORDER POLE STAGE

Noise Simulation

The ISL28133 input current noise is very small (~70fA), so it is neglected in this model. The voltage noise of the MOSFET can be modeled like the following equations.

$$V_i^2(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_m} + \frac{K}{WLC_{ox}f} \quad \text{(EQ. 5)}$$

$$g_m \propto \sqrt{I_D} \quad \text{(EQ. 6)}$$

I_D is the drain current. High bias current in the model is needed to emulate the low voltage noise. At the input stage, the tail current is set high enough to generate the low input voltage noise. Before the noise sources are added, the model has to be rendered lower noise than the spec or typical performance noise curve in the datasheet. The noise-voltage module of Figure 6 generates 1/f and white noise by using a 0.1V voltage source biasing a diode-resistor series combination. White noise is generated by the thermal noise-current.

$$i_n^2 = \frac{4kT}{R} \quad \text{(EQ. 7)}$$

where k is the Boltzmann's constant. So, the required value of the resistor for a given noise-voltage spectral density is:

$$R = \frac{e_n^2}{2 \times 4kT} \quad \text{(EQ. 8)}$$

where e_n is the spectral density of the white noise voltage. The design of the chopper stabilized amplifier greatly reduced 1/f noise. 1/f noise (flicker noise) refers to the noise exhibiting power spectral density inversely proportional to the frequency. More generally, the noise with the spectral density

$$S_N \propto \frac{1}{|f|^\beta} \quad \beta > 0 \quad \text{(EQ. 9)}$$

is also called 1/f noise. Normally, the frequency where the flicker noise curve crosses the white noise curve is defined as the corner frequency. The small amount of flicker noise that remains is modeled within the SPICE diode model. Referring to Figure 6,

$$i_n^2 = 2qI_d + KF \bullet \frac{I_d^{AF}}{frequency} \quad \text{(EQ. 10)}$$

Id is the DC diode current. AF and KF are the model parameters of the SPICE diode and q is the charge of the electron. The flicker noise exponent (AF) is set to 1 and the flicker noise coefficient (KF) is set

$$KF = \frac{E_a^2}{2R^2 \bullet I_d} \quad \text{(EQ. 11)}$$

where Ea is the noise-voltage spectral density at 1Hz. The simulated voltage noise will show the 1/f noise-voltage spectral density with the correct corner frequency.

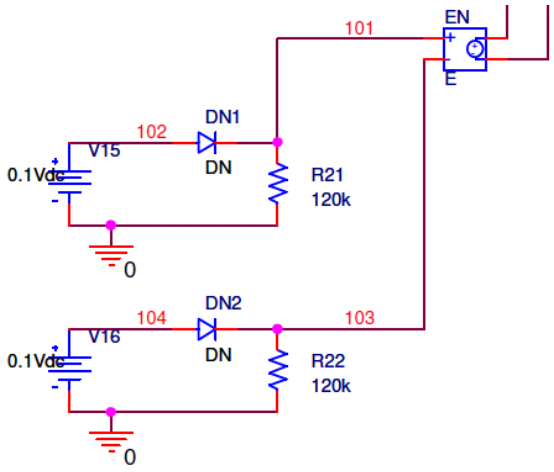

FIGURE 6. NOISE VOLTAGE MODULE

Output Stage

After the frequency shaping-stages, the signal appears at Node VV5, which is referenced to the midpoint of two supply rails. Each controlled source can generate enough current to support the desired voltage drop across its paralleled resistor. R15 and R16 are equal to twice of the open loop output resistance, so their parallel combination gives the correct Zout. D5-D8 and G9/10 are used to force a current from the positive rail to the negative rail to correct the real current sink or source in the supply pins.

$$G9 = G10 = G11 = G12 = \frac{1}{2Z_{out}} \quad \text{(EQ. 12)}$$

$$R15 = R16 = 2Z_{out} \quad \text{(EQ. 13)}$$

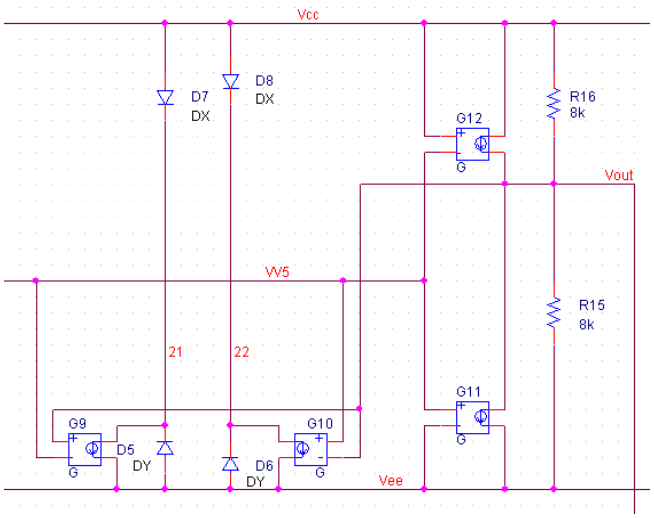

FIGURE 7. OUTPUT STAGE

Simulation Results

Some SPICE simulation results are compared with the typical performance curve from the datasheet in the following. (Figure 8b is from the datasheet).

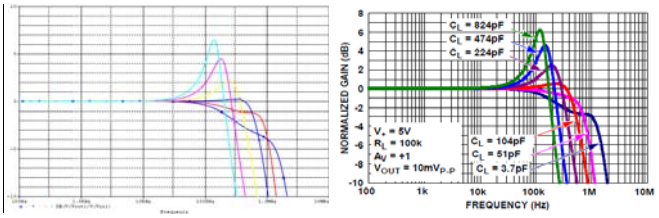

FIGURE 8. GAIN vs FREQUENCY vs LOAD CAPACITANCE. IT CANNOT BE VERY ACCURATE BECAUSE THE PARASITIC CAPACITANCE ON THE BOARD WASN'T INCLUDED IN THE MODEL. THE ERROR IS LESS THAN 5%

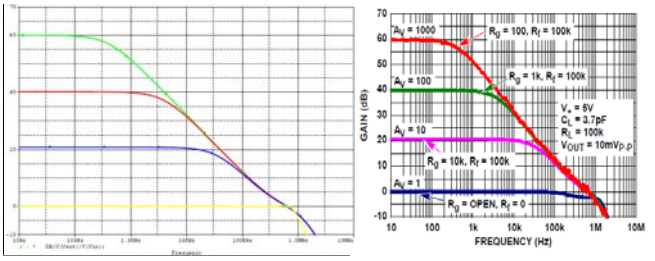

FIGURE 9. FREQUENCY RESPONSE OF CLOSED LOOP GAIN WITH DIFFERENT GAIN. AT GAIN = 100, THE BANDWIDTH IS 3.94kHz AND THE ERROR IS LESS THAN 5%. AT LOW GAIN, THE BANDWIDTH IS EXPANDED BECAUSE OF THE ZERO POLE PAIR

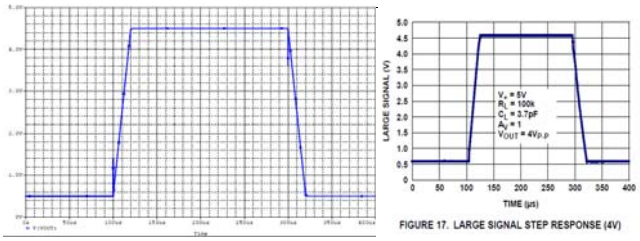

FIGURE 10. LARGE SIGNAL STEP RESPONSE. THE SLEW RATE SIMULATED IS 0.198V/µs AND THE ERROR IS 1%

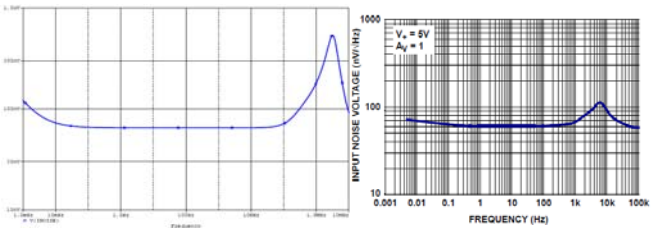

FIGURE 11. INPUT NOISE VOLTAGE vs FREQUENCY. AT 1kHz, THE SIMULATED INPUT NOISE VOLTAGE IS 64.9 nV/Hz, VERY CLOSE TO THE VALUE IN THE DATASHEET 65nV/Hz. THE SIMULATED CURVE CANNOT CATCH THE PEAK NEAR 10kHz

Conclusion

A truly comprehensive SPICE macromodel for a voltage feedback amplifier is developed. This macromodel includes effects such as transfer response, accurate AC response, DC offset and voltage noise. It is easy to add more features like CMRR, PSRR, input current-noise, etc. Also it is convenient to change the parameters of the model to fit other voltage feedback amplifiers. Actually, several of Intersil's voltage feedback amplifiers use the same model topology.

ISL28133 Macromodel Netlist

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* ISL28133 Macromodel

* Revision B, July 2009 by Jian Wang

* This model simulates AC characteristics, Voltage Noise,
Transient Response

* Connections: +input -input +Vupply -Vsupply Vout

.subckt ISL28133      3      2   7     4       6

*Input Stage

C_Cin1       8 0  1.12p

C_Cin2       2 0  1.12p

C_Cd         8 2  1.6p

R_R1        9  10  10

R_R2        10 11  10

R_R3        4  12  100

R_R4        4  13  100

M_M1        12 8 9 9   pmosisil

+ L=50u
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```
+ W=50u
M_M2      13 2 11 11 pmosisil
+ L=50u
+ W=50u
I_I1      4 7 DC 92uA
I_I2      7 10 DC 100uA
*Gain stage
G_G1      4 VV2 13 12 0.0002
G_G2      7 VV2 13 12 0.0002
R_R5      4 VV2  1.3Meg
R_R6      VV2 7  1.3Meg
D_D1      4 14 DX
D_D2      15 7 DX
V_V3      VV2 14 0.7Vdc
V_V4      15 VV2 0.7Vdc
*SR limit first pole
G_G3      4  VV3 VV2 16 1
G_G4      7  VV3 VV2 16 1
R_R7      4 VV3  1meg
R_R8      VV3 7  1meg
C_C1      VV3 7  12u
C_C2      4 VV3  12u
D_D3      4 17 DX
D_D4      18 7 DX
V_V5      VV3 17 0.7Vdc
V_V6      18 VV3 0.7Vdc
*Zero/Pole
E_E1      16 4 7 4 0.5
G_G5      4  VV4 VV3 16 0.000001
G_G6      7  VV4 VV3 16 0.000001
L_L1      20 7   0.3H
R_R12     20 7  2.5meg
R_R11     VV4 20  1meg
L_L2      4  19  0.3H
R_R9      4  19  2.5meg
R_R10     19 VV4  1meg
*Pole
G_G7      4 VV5 VV4 16 0.000001
G_G8      7 VV5 VV4 16 0.000001
C_C3      VV5 7  0.12p
C_C4      4 VV5  0.12p
R_R13     4 VV5  1meg
R_R14     VV5 7  1meg
*Output Stage
G_G9      21 4 6 VV5 0.0000125
G_G10     22 4 VV5 6 0.0000125
D_D5      4 21 DY
D_D6      4 22 DY
D_D7      7  21 DX
D_D8      7  22 DX
R_R15     4 6  8k
R_R16     6 7  8k
G_G11     6 4 VV5 4 -0.000125
G_G12     7 6 7 VV5 -0.000125
*Voltage Noise
D_DN1     102 101 DN
D_DN2     104 103 DN
R_R21     0 101  120k
R_R22     0 103  120k
E_EN      8 3 101 103 1
V_V15     102 0 0.1Vdc
V_V16     104 0 0.1Vdc
.model pmosisil pmos (kp=16e-3 vto=10m)
.model DN D(KF=6.4E-16 AF=1)
.MODEL DX D(IS=1E-18 Rs=1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28133
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References

[1] BOYLE, G.R., "Macromodeling of integrated circuit operational amplifiers", IEEE J. 1974, SC-9.

[2] Derek Bowers, Mark Alexander, Joe Buxton, "A Comprehensive Simulation Macromodels for 'Current Feedback' Operational Amplifiers," IEEE Proceedings, Vol. 137, April 1990 pp.137-145

[3] Mark Alexander, Derek Bowers, "AN-138 SPICE-Compatible Op Amp Macro-Models", Analog Devices Inc., Application Note 138.

[4] "AN-840 Development of an Extensive SPICE Macromodel for 'Current-Feedback' Amplifiers", National Semiconductor Corp., Application Note 840.